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| 10/706,195 | 11/12/2003 | Raju Yasala | 30320/17230 | 5989 |

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| EXAMINER | |
|---|---|
| WEST, JEFFREY R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2857 | |

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/706,195 | YASALA, RAJU | |
| | Examiner | Art Unit | |
| | Jeffrey R. West | 2857 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement filed March 19, 2004, fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement.

2. The information disclosure statement filed March 19, 2004, fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

### *Drawings*

3. The drawing in Figure 1 is objected to because it does not have sufficiently

descriptive labels. Blank boxes in drawings should be labeled descriptively unless it is a well-known component.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

5. The abstract of the disclosure is objected to because its length is less than the required 50 words. Correction is required. See MPEP § 608.01(b).

6. The disclosure is objected to because of the following informalities:

Page 4, paragraph 0015, lines 3-4, describes "connecting the current sensor 145 to the target processor 115", however, Figure 1 illustrates that the current sensor is connected to input "140" of host system "100" and not the target processor "115".

Appropriate correction is required.

***Claim Objections***

7. Claims 1, 18, and 20 are objected to because of the following informalities:

In claim 1, line 1, "For a processor having a power line, a system to determine" should be ---A system, for a processor having a power line, to determine---.

In claim 18, lines 1-2, "For a target processor including a power line, a system to determine" should be ---A system, for a target processor including a power line, to determine---.

In claim 18, line 4, to avoid problems of antecedent basis, "the magnitude" should be ---a magnitude---.

In claim 18, line 7, to avoid confusion, "of current by the target processor" should be ---of current---.

In claim 20, line 8, to avoid problems of antecedent basis, "the parameters" should be ---the parameter---.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,304,978 to Horigan et al.

With respect to claims 1 and 22, Horigan discloses a system, for a processor having a power line, to determine processor utilization, the system comprising a sensor ("255") coupled to the power line ("247") for measuring a current magnitude in the power line as the current being consumed by the processor (column 5, lines 45-47 and Figure 2).

10. Claims 1-8 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,721,672 to Spitaels et al.

With respect to claims 1 and 22, Spitaels discloses a system, for a processor having a power line, to determine processor utilization (column 6, lines 18-21), the system comprising a sensor coupled to the power line for measuring a current

magnitude of the power line indicating current being consumed by the processor (column 6, lines 35-39).

With respect to claims 2, 7, 8, and 23 Spitaels discloses that the measured current is compared to a maximum current value indicative of current consumed by the processor when fully utilized to insure that the maximum current is utilized (column 8, lines 48-55 and column 9, lines 43-52) using a software application means (column 5, lines 61-64).

With respect to claims 3, 4 and 24, Spitaels discloses using a software application (column 8, lines 35-38) to determine a maximum current value indicative of current consumed by the processor when fully utilized (column 8, lines 50-58).

With respect to claim 5 and 6, Spitaels discloses using a software application to cause the processor to be fully utilized (column 6, lines 3-4 and 10-21).

### *Claim Rejections - 35 USC § 103*

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-8, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horigan in view of U.S. Patent No. 6,721,672 to Spitaels et al:

As noted above, the invention of Horigan teaches many of the features of the claimed invention and while Horigan also discloses a software application means

that compares the measured current to a maximum current threshold (column 6, lines 14-25) as well as a means for adjusting the utilization of the processor according to the threshold level using a software application (column 6, lines 40-52), Horigan does not specifically indicate that the maximum current threshold is a maximum current indicative of a current consumed by the processor when fully utilized.

Spitaels teaches a system wherein a measured current is compared to a maximum current value indicative of current consumed by the processor when fully utilized to insure that the maximum current is utilized (column 6, lines 3-4 and 10-21, column 8, lines 48-55 and column 9, lines 43-52) using a software application means (column 5, lines 61-64). Spitaels also teaches using a software application to cause the processor to be fully utilized (column 6, lines 3-4 and 10-21).

It would have been obvious to one having ordinary skill in the art to modify the invention of Horigan to include specifying that the maximum current threshold is a maximum current indicative of current consumed by the processor when fully utilized, as taught by Spitaels, because, as suggested by Spitaels, the combination would have insured that the processor operated a level of full optimization thereby increasing the efficiency of the processor by allowing it to correctly run a maximum amount of tasks (column 5, line 64 to column 6, line 6 and column 6, lines 18-29)

13. Claims 9-16 and 18-21 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Spitaels et al. in view of U.S. Patent No. 6,057,839 to Advani et al.

As noted above, the invention of Spitaels teaches many of the features of the claimed invention and while the invention of Spitaels does teach means for adjusting the utilization of the processor to be fully utilized, Spitaels does not explicitly teach the means for calculating the utilization of the processor. Further, Spitaels does not specifically include means for displaying the utilization of the processor.

Advani teaches a visualization tool for graphically displaying trace data produced by a parallel processing computer comprising a host including a host processor and host memory storing a utilization utility adapted to be stored in the host memory and executed by the host processor (column 4, lines 46-64), the utilization utility further adapted to calculate utilization information of a target processor (column 5, lines 51-57) as well as generate a graphical representation of the processor utilization (column 5, lines 58-60) to optimize a software application executing on the target processor in response to the calculated target processor utilization information (column 2, lines 15-20).

It would have been obvious to one having ordinary skill in the art to modify the invention of Spitaels to explicitly teach the means for calculating the utilization of the processor and a corresponding means for displaying the utilization of the processor, as taught by Advani, because, as suggested by Advani, the combination would have improved the processor operation by displaying the data in an easily understandable

format for real time debugging and analysis of computing interactions (column 1, lines 25-32).

14. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spitaels et al. in view of Advani et al. and further in view of U.S. Patent No. 4,823,075 to Alley.

As noted above, the invention of Spitaels and Advani teaches many of the features of the claimed invention and while the invention of Spitaels and Advani do teach a current sensor for sensing a current consumed by a processor, the combination does not specifically indicate that the sensor is a Hall-effect sensor.

Alley teaches a current sensor using a Hall-effect device with feedback including a Hall-effect sensor for sensing the current (column 2, lines 16-39).

It would have been obvious to one having ordinary skill in the art to modify the invention of Spitaels and Advani to specify that the current sensor be a Hall-effect sensor, as taught by Alley, because Alley suggests that the combination would have provided a well-known, accurate, less expensive sensor applicable to the invention of Spitaels and Advani while minimizing the space required for the sensor (column 2, lines 3-8).

## *Conclusion*

15. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 6,636,976 to Grochowski et al. teaches a mechanism to control di/dt for a microprocessor.

U.S. Patent No. 6,457,131 to Kuemerle teaches a system and method for power optimization in parallel units.

U.S. Patent No. 6,105,142 to Goff et al. teaches an intelligent power management interface for computer system hardware.

U.S. Patent No. 5,692,204 to Rawson et al. teaches a method and apparatus for computer system power management.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
February 17, 2005